IN THE CLAIMS

Please amend the Claims as follows.

10. (Currently Amended) A split-gate flash memory structure, comprising:

a substrate having a trench therein;

a floating gate formed inside the trench, wherein the upper surface of the floating gate is lower than the upper surface of the substrate;

a tunnel oxide layer formed between the floating gate and the substrate;

a select gate formed inside the trench, wherein the upper surface of the select gate is protruding beyond the upper surface of the substrate; ~~and~~

a gate dielectric layer formed between the floating gate and the select gate;

a dielectric layer formed between the select gate and the substrate, wherein a portion of the dielectric layer is physically in contact with a sidewall of the trench and the select gate; and

a source/drain region formed on each side of the select gate in the substrate, wherein the source/drain region and the floating gate are separated from each other by a distance.

Claim 11 (canceled).

Claim 12 (canceled).

Claim 13 (canceled).

14. (Currently Amended) The split-gate memory of claim ~~12~~10, wherein the gate dielectric layer includes an oxide/nitride/oxide composite layer.

15. (Currently Amended) The split-gate memory of claim ~~12~~10, wherein the structure further includes a lightly doped region formed between the source/drain region and the select gate.

16. (Currently Amended) The split-gate memory of claim ~~12~~10, wherein the structure further includes a spacer formed on sidewalls of the select gate.

17. (New) The split-gate memory of claim 16, wherein the spacer includes silicon oxide or silicon nitride.

18. (New) The split-gate memory of claim 10, wherein the dielectric layer includes silicon oxide.

19. (New) The split-gate memory of claim 10, wherein the select gate comprises a doped polysilicon layer.